Design of a programmable CMOS Charge-Pump for phase-locked loop synthesizers

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Abstract: A charge pump circuit capable of operating at different switching speed is presented. The switching speed control is added to a typical charge pump circuit by mean of enable switches which allow to drive different currents. Charge pump circuit is implemented in AMI 0.5um CMOS technology. Simulations were performed using Spectre from Cadence. Simulation results show clearly an increase in the slope of charging or discharging curves of load capacitor during the pumping-up and pumping-down phases.

Keywords: analog electronic design; integrated circuits; charge pump; PLLs; circuit simulation.

Introduction

Charge-pump (CP) circuit is a building block of A/D and D/A converters, dynamic random access memory circuits, switched-capacitor circuits and phase locked loop (PLLs). In a PLL system CP circuit consists of switched current sources which generate up and down current pulses to adjust voltage controlled oscillator (VCO) control voltage on filter capacitor. Three important issues of on-chip CP circuits are output voltage ripple, power efficiency and area efficiency [1]. Because large output ripple degrades the performance of the circuit that the CP is powering, for most applications, a low output ripple is desired. CPs with very low power efficiency cancel the benefit of scaling the supply voltage down and are not desirable for portable applications. Area efficiency is desirable for many applications as smaller chip areas are less expensive to fabricate. Among different PLL topologies, charge-pump phase locked loop (CPPLL) is widely used in modern wireless communication systems due to the phase-lock advantages, namely their larger system gain, faster frequency detecting reactions, larger range acquisition and a perfect zero static phase error [2], and also offering programmability features, this last allowing to satisfy the needs set by modern RF reconfigurable systems, able to work under different protocols & standards. An ideal CPPLL model has a perfect zero input phase error, but taking the mismatch into account, certain phase error is introduced in practical circuits. That means the matching precision of CP is directly related to the phase error of the whole PLL system. Non ideal behavior of CP can contribute significantly to PLL output jitter [2, 3] and precision of A/D, D/A converters and switched capacitor filters is affected by the switch-induced error voltage. Non idealities come mainly from charge sharing, charge injection and clock feedthrough in MOS analog switches of CPs, so transistors' switch sizing is a key design variable in order to get best performance of CPs. Different approaches to the reduction of the switch induced error have been proposed in references [4 – 12]. In a PLL system, if phase detector circuit perceives change in phase, it provides information to CP which converts phase error information into current to generate control voltage of VCO. Up (down) CP current pulses lead to charge (discharge) the filter capacitor. The voltage step during the charge (discharge) is directly related with CP current, then by controlling the magnitude of CP current one could control the charge/discharge speed of filter capacitor and this offers an effective way of enable PLL operation at different frequencies. In this work, a charge-pump topology with two current levels is presented. Design approach of CP circuit is described in section III. In section IV, simulation results will be given. Finally, the conclusion is drawn in section V.

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Charge-pump circuit

A block diagram of a CPPLL synthesizer system is illustrated in Fig. 1. From this figure, one can note five main blocks: phase /frequency detector (PFD), charge-pump (CP), low pass filter (LPF), and voltage controlled oscillator (VCO) and frequency divider. Among them, the CP consists of two switched current sources that pump charge into or out of the LPF according to the output signal from the PFD. I1 is designed as charging current (I_{UP}) whereas I2 is identified as a discharging current (I_{DW}), and they are nominally equal. Basic operation is as follows: if QA = QB = 0, S1 and S2 are open and Vctrl remains constant. If QA = 1 and QB = 0, then S1 closes whereas S2 is open and I_{UP} charges the filter capacitor (Cp). Conversely, if QA = 0 and QB = 1, S2 closes and S1 opens, then I_{DW} discharges Cp. Thus, if for instance, Vout lags Vin, QA continues to produce pulses and Vctrl rises steadily towards VDD.

From dynamic behavior of CPPLL the relationship between Vctrl, I_{UP} (I_{DW}) and phase difference $\Delta\phi$ is deduced as follows [11]:

$$V_{ctrl}(t) = \frac{I_{UP}T_{in}}{2\pi C_P}\Delta\phi = \frac{I_{UP}\phi_0}{4\pi f C_P} \qquad (1)$$

This means that Vctrl rises in steps proportional to the ratio I_{UP}/C_P every period Tin (see Fig. 2). As an example, suppose a 10MHz clock frequency, a Cp = 5pF, and I_{UP} = 10uA, the resulting voltage step height is 100mV. As Eq. 1 reveals if one doubles I_{UP}, the slope of Vctrl vs t curve should be doubled, that is, the voltage step height now is 200mV. Thus we can take advantage of this behavior to adjust the speed for charging or discharging filter capacitor [12]. In other words, we can utilize I_{UP} current as an extra variable control to set up the speed response of the PLL system.
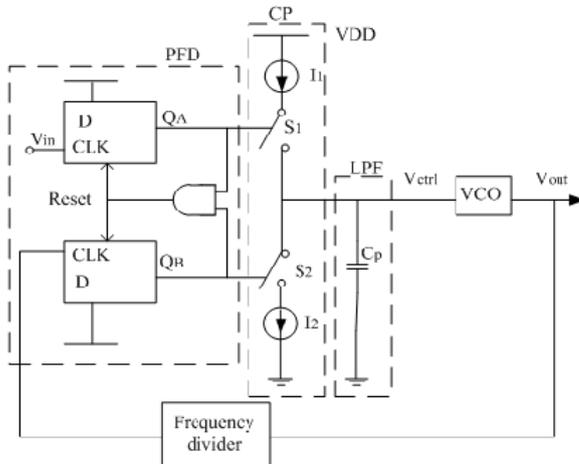

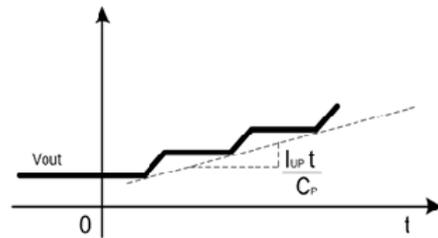
Fig.1: typical CPPLL synthesizer system.   Fig. 2: step response of CPPLL synthesizer.

Proposed charge-pump circuit

Conceptual representation of CP circuit in which magnitude currents I_{UP} (I_{DW}) can be adjusted is shown in Fig. 3a. Traditional CP circuit is composed by S1, S2 switch array and transistors MB1, MB2, MB4 MB5, and MB7. MB1 sets I_{UP} (I_{DW}) current through current source composed by MB2, and MB4 (MB5 and MB7). In order to provide CP circuit an option to drive different I_{UP} (I_{DW}) current, enables switches are implemented (Fig. 3b). Basic principle of operation is as follows: when enable signal is applied "enab_b" switch is closed and transistor MB6 turns-on. If MB6 and MB7 are equally sized I_{UP} current is doubled and consequently the charge speed of filter capacitor is doubled. This also holds for the complementary part, i.e., I_{DW} doubling current when MB3 is turned-on by closing "enab". The "enable" switch is composed by transistors Me1 and Me2 while Me3 and Me4 forms switch "enab_b". Switches S1 and S2 were implemented with transmission gate topology in order to minimize injection current and clock feedthrough phenomena. The whole circuit is presented in fig. 3b. Transistor MB1, MB2, MB3, MB4 MB5, MB6 and MB7 were sized in order to drive 10uA DC current (Eq. 2) whereas MS1 to MS4 were sized in terms of 1kΩ of on-resistance switches (Eq. 3). Me1 to Me4 transistors were sized to set a V_G voltage of MB6 (MB3) 100mV higher than

V_{TH}. Process parameters i.e., V_{TH}, KP, λ, etc., were extracted by Spectre simulations using AMI C5N technology. Table 1 summarizes the transistor dimensions of CP circuit shown in Fig. 3. Notice the reduced number of transistors as well as their small dimensions implies low area in layout.
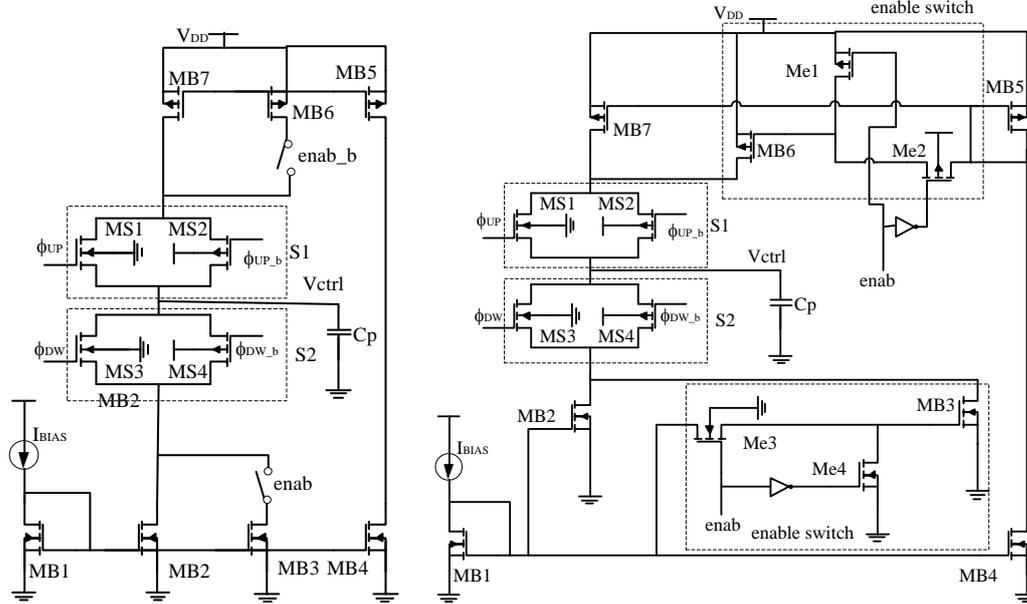

Fig.3: (a) Conceptual representation of CP circuit for driving different I_{UP} (I_{DW}) currents, (b) Final charge pump schematic approach.

$$I_D = \frac{1}{2}kP\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \tag{2}$$

$$R_{ON} = \frac{1}{kP\dfrac{W}{L}\left(V_{GS} - V_{TH}\right)} \tag{3}$$

Table 1: Charge Pump circuit parameter

Block	Transistor	W (um)	L (um)
Bias	MB1, MB2, MB3, MB4, MB5, MB6, MB7	$2.1_{MB1,2,3,4}$ $3.3_{MB5,6,7}$	1.2
S1 switch	MS1, MS2	1.5	0.6
S2 switch	MS3, MS4	1.65	0.6
I_{UP} enable switch	Me1, Me2,	1.5	0.6
I_{DW} enable switch	Me3, Me4,	1.5	0.6

Simulation results

Transient simulations have been performed using a 0.5µm CMOS process from AMI C5N technology provided by MOSIS and Spectre simulator provided by Cadence[TM]. Fig. 4a presents a closed up image during the pumping-up phase for the two I_{UP} current levels. As can be noticed from Fig. 4a, the step sizes of Vctrl are quite matched with model given by Eq. 1, that is, step size doubles when I_{UP} is doubled. Similar behavior was observed during the pumping-down phase (Fig. 4b). Also a higher slope can be observed for the charge intervals in the whole pumping up or pumping down phase (Fig. 4c) which validates this approach.
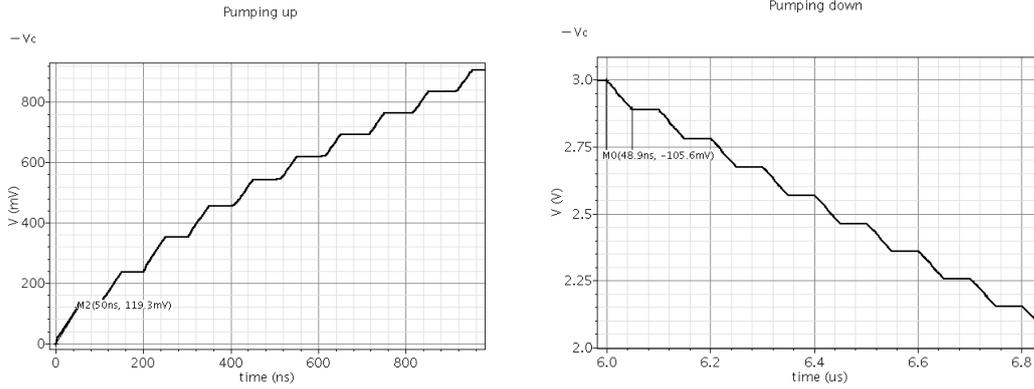
Fig. 4: Simulation results of proposed charge pump circuit (VDD = 3V, f= 10MHz): (a) Pumping-up, (b) pumping down.
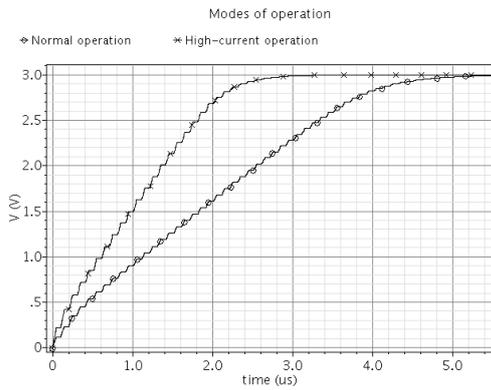

Fig.5: Charge pump simulation results.

Conclusions

This paper proposed a new structure of high performance CMOS charge pump for phase-locked loop synthesizer. According to the test results, with the help of enable switch added to the traditional charge pump circuit I_{UP} (I_{DW}) current can be chosen to fix the charge/discharge speed of filter capacitor. The proposed CP has a wide current match range, a high matching precision. This CMOS charge pump structure can be applied in a CPPLL with high performance.

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