Comparison of conventional and new class AB modifications of the Flipped Voltage Follower and their implementation in high performance amplifiers

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***Abstract*—A comparison between different modifications of the conventional cell denominated as Flipped Voltage Follower to provide class AB operation is presented. Additionally, two new class-AB structures with high linearity and large operational range are introduced, and included in the comparison. Computer simulation shows the operation of these modifications when driving a capacitive load, including the resulting output resistance when the class AB operation is achieved. Also, the implementation of these modifications in a highly linear operational transconductance amplifier is discussed, as well as the impact of the output resistance of these modifications on the linearity of the system. Additionally, a variation of conventional cascoded current mirrors used in the amplifier to achieve very large output currents is presented. Simulation results in 0.5µm technology show the results of the comparison.**

I. INTRODUCTION

Many architectures and modifications to achieve high performance voltage followers have been reported recently. Specifically, the denominated Flipped Voltage Follower (FVF) [1] shown in Fig. 1a has been object of study for many authors in the past few years. It consists of two transistors and a biasing current source, where transistor M2 adopts a constant biasing current I_B, and due to the shunt feedback M1 is able to sink large currents. A signal current induces variations in the gate-source voltage of this transistor v_{gs1}, which are attenuated by M2 at the output node by a factor $g_{m2}r_{o2}$, thus resulting in a very low output resistance of $\sim 1/g_{m1}g_{m2}r_{o2}$. This low resistance has been motive to implement this basic cell in many applications such as in differential pairs and current mirrors for operational transconductance amplifiers (OTA). However it presents considerable limitations such as limited output swing of $V_o^{swing} = V_{GS1}\text{-}V_{DS2}^{sat}\text{-}V_{DS1}^{sat}$, a possible solution to overcome this is found in [2]. Additionally, the intention to adapt this cell to provide large currents in both directions and have class AB operation has resulted in the invention of many variations reported in the past [3]-[6]. In this paper we present a comparison between the different variations of the FVF, advantages and disadvantages, and their implementation in an OTA to offer high performance operation.

II. CLASS AB OPERATION OF VOLTAGE FOLLOWERS

A. Class AB modifications of the FVF

The conventional FVF in Fig. 1a has the property of sinking large currents, although it's sourcing capability is limited to I_B, thus the modifications discussed in this section present an alternative to provide the ability to source large currents.

The first structure shown in Fig. 1b was reported by Ramirez-Angulo et.al. in [3]. A capacitor C_{bat} and a transistor operating as a large resistor R_{large} are included. Under static conditions the circuit is biased through R_{large} similar to the conventional FVF, however under dynamic conditions the capacitor cannot charge/discharge rapidly due to the large resistor, and forms a constant voltage that functions as a battery that provides push-pull behavior proper to class AB operation. It provides large swing for both M1 and the transistor represented as R_L. However, it presents two main limitations, first, the capacitor discharges after some time, losing its property of a floating battery and the current sourcing capability. Second, the sourcing current provided by M_L passes through M2, hence affecting the gate-source voltage V_{GS2} and varying the output voltage with respect to the input signal. This results in an output resistance defined by M2 as $1/g_{m2}$ instead of the desired low resistance $1/g_{m1}g_{m2}r_{o2}$ as in the case of the conventional FVF, also decreasing the speed of operation.

The second modification is shown in Fig. 1c and reported by Jimenez et.al in [4]. In this scheme an additional NMOS

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transistor M3 is connected in parallel with the input transistor M2. Here the largest current to be sourced by M2 is I_B, when this situation is reached this transistor is unable to provide a larger current, thus entering deeply in triode region of operation, where M3 is then able to provide larger currents as needed. The limitations of this architecture rely on the fact that when M3 is providing current the output voltage depends on the voltage V_{GS3} with respect to V_i, similar to the previous case of circuit in Fig. 1b, where also the output resistance results in $1/g_{m3}$ which, again, is not as low as the desired resistance in the conventional FVF.

The third modification is shown in Fig. 1d and reported by Centurelli et.al. in [5]. In this case the current in M3, through the path of the unity-gain inverter, is sensed by M4 and compared to the reference I_B at node *b*. This comparison defines the gate-source voltage of M1 and thus the current in that path. For a current to be sank at the output node, the current in M1 increases, and the conditions in M3 remain unchanged; however under the sourcing condition the current in M3 increases, and the current comparison at node *b* simply turns M1 off. A disadvantage of this scheme is that the sourcing current passes through M2, thus the output voltage depends on V_{GS2}, again limiting the output resistance to 1/gm2. Additionally, large sourcing currents are copied to M_{invP}, thus consuming twice the current and increasing power dissipation, which in fact is also increased under static conditions as two more paths are included.

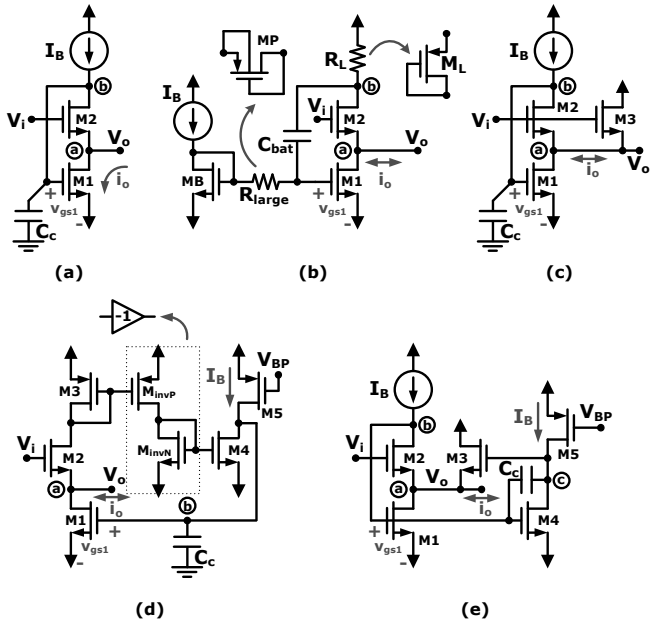

Figure 1. Voltage followers: a) conventional class A FVF in [1], b) Class AB version by Ramirez-Angulo [3], c) Class AB version by Jimenez [4], d) Class AB version by Centurelli [5], and e) Class AB version by Padilla-Cantoya [6].

The fourth modification is shown in Fig. 1e and reported by Padilla-Cantoya et.al. in [6]. In this structure the current in M1 is compared to I_B by means of M4 at node *c*; this comparison is then used to control the channeling of M3. In case a large current is required to be sourced the gate-source voltage of M1 decreases, resulting in M4 to increase the gate-source voltage of M3 as much as it is required so as to keep the current in M1 equal to I_B. Note that, contrary to the other cases, the transistor operating as voltage follower M2 maintains a constant current, which results in conservation of a low output resistance defined by $1/g_{m3}g_{m2}r_{o2}g_{m4}r_{o4}$.

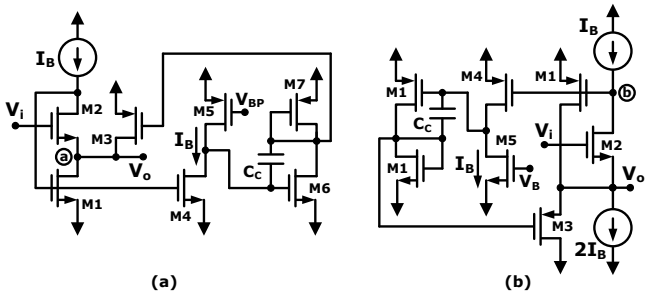

Figure 2. Proposed class AB voltage followers based on the modification of the FVF in a) Padilla-Cantoya [6], and b) its extended output-swing version.

B. *Proposed structures*

As mention earlier, the sourcing current in Fig. 1e is provided by M3, hence, for a large current the gate-source voltage in this transistor has to increase. This is present when the circuit is sourcing current, although under this condition the output voltage increases, thus creating the undesired tendency of reducing V_{GS3} instead of increasing, limiting its voltage swing and hence, the current sourcing capability. This can be avoided by using a p-type transistor for the sourcing effect, as shown in Fig. 2a. In this case the output is connected to the drain terminal of M3, thus, the gate and source terminals are independent from the output node. Note that an additional unity-gain stage is required to achieve negative feedback due to the counter part replacement of M3. Straight forward analysis shows that a capacitor C_c is required for frequency compensation of the same value as that in Fig. 1a and Fig. 1e, $C_c > C_L/g_{m2}r_{o2}$ as reported in [1] and [6].

This topology has the same output swing limitation as circuits in Fig. 1a, 1c, and 1e, defined as $V_o^{swing}=V_{TH}-V_{DS2}^{sat}$. Therefore, an increased-output-swing version of the proposed circuit is depicted in Fig. 2b, which is based on the Folded Flipped Voltage Follower (FFVF) reported in [7], [8] and offers an output swing of $V_o^{swing}=V_{dd}-V_{ss}-V_{GS1}-2V_{DS}^{sat}$, where the rails can be adjusted as needed.

C. *Implementaiton in a highly linear V-I converter*

In order to observe the benefits of these cells they were implemented in a high performance operational transconductance amplifier (OTA) reported in [9] (and [10] using the FFVF). This high performance OTA, shown in Fig. 3, exhibits very high linearity by making use of the very low output resistance of the conventional FVF. Differential input signals are reflected at nodes *a* and *b* level shifted by $V_{GS2,4}$; this creates a voltage drop across resistor R inducing a current I_R, and thus varying the currents in the transistors M1 and M3. The resulting gate-source voltages in these transistors produce differential currents which by means of the cascoded current mirrors are added at output node to offer single-ended operation. Note that the maximum current to be provided at

the output node is $2I_B$. Thus, the FVF cells marked in dashed squares were replaced with the variations previously discussed as shown in Fig. 2b so as to increase the output current, resulting in highly linear Class AB OTA's (the actual implementation of the modifications is not shown for the sake of space).

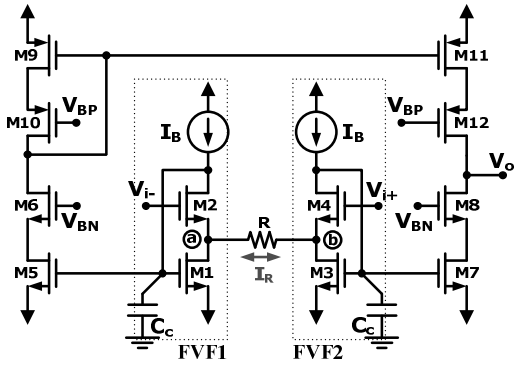

Figure 3. Highly linear V-I converter with conventional FVF usded to test the performance of circuits in Fig. 1b-1d and proposed structure in Fig. 2a.

As class AB circuits large currents are supported, hence, large drain-source saturation voltages of transistors in the current mirrors are expected, thus the cascoding voltages have to be large enough to allow this increment. Therefore, a modification to the current mirror is also presented, as shown in the schematic, comprised by transistor M_{LS} and an additional current source, which includes an additional gate-source voltage drop, thus increasing the operational range of the saturation voltages of these transistors. This modification is equivalent to the level shift version of the FVF presented in [2] as LSFVF.

III. SIMULATION RESULTS

Computer simulations where performed on spectre using 0.5µm double-poly three-metal CMOS technology. The nominal threshold voltages are V_{THN} = 0.7 V and V_{THP} = -0.9 V for NMOS and PMOS respectively. Transistor sizes are 43.8/1.2 and 126.6/1.2 µm/µm for NMOS and PMOS respectively. The circuit was tested with a supply voltage of V_{dd} = -V_{ss} = 2 V and a biasing current I_B = 30 µA. These values, in combination with the technology parameters, result in a saturation voltage for all the transistors of approximately V_{DS}^{sat} = 0.2 V. For the cascoding voltages the values V_{CN} = 1.4 V and V_{CP} = 1.6 V were used.

Fig. 4 shows the simulated transient characteristic of the conventional and proposed voltage followers in Fig. 1e and 2a respectively, when driving a 1kΩ load resistor. Note that in the case of the conventional follower, the reduced swing in M3 results in a limited sourcing current when the circuit is slewing positively, hence distorting the output signal; whereas the proposed circuit is capable to drive low resistive loads.

TABLE I. DESIGN PARAMETERS OF FVF'S IN FIG. 1.

FVF in Figure	*R_o (when sourcing current)*	*Minimum supply voltage*	*Supply current*
Fig. 1b	$1/g_{m2}$	$V_{GSN}+V_{GSP}$	I_B
Fig. 1c	$1/g_{m3}$	$V_{GSN}+V_{DS}^{sat}$	I_B
Fig. 1d	$1/g_{m2}$	$V_{GSP}+2V_{DS}^{sat}$	$3I_B$
Fig. 2a	$1/g_{m3}g_{m2}r_{o2}g_{m4}r_{o4}$	$V_{GSN}+2V_{DS}^{sat}$	$2I_B$

Table I shows a comparative analysis on the output resistance, minimum supply voltage and supply current of the voltage followers. Fig. 5 shows the dc transfer characteristic of the V-I converter in Fig. 2b when implementing the followers under discussion. Note that when using the circuits in Figs. 1c and 1d and a large current is being demanded the output resistance changes thus affecting the transconductance dramatically, also introducing undesired nonlinearity. Additionally, when using the circuit in Fig. 1b, despite the fact that the transconductance is lower due to the output resistance, it has a linear response over the entire operational range. Observe that the circuit in Fig. 2a (similar to that in Fig. 2b) provides a linear response without reducing the transconductance.

Fig. 6 shows the transient response of the converter when driving a capacitor C_L = 15 pF with a square input signal of $0.5V_{pp}$ at 2MHz and a resistive load R_L = 1kΩ with a sine wave input signal of $0.5V_{pp}$ at 10 kHz. The response for the square signal is similar to that of the followers in Fig. 4; the slew rate results are shown in Table II. Also, the linearity is shown in the table for the sine input signal.

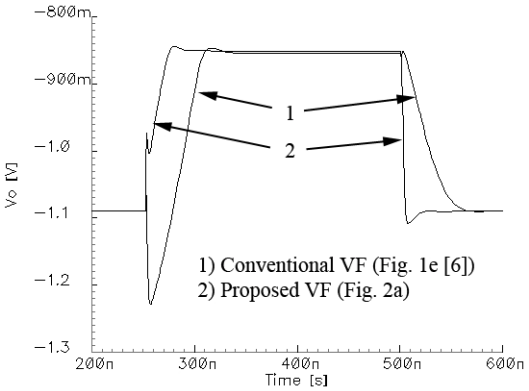

Figure 4. Transient response of the conventional and proposed voltage followers in Fig. 1e and 2a respectively, for an input signal of $300mV_{pp}$ at 2MHz with a load resistor of 1kΩ.

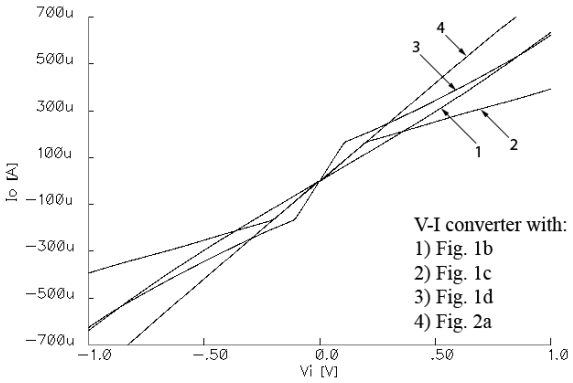

Figure 5. Dc transfer characteristic of the V-I converter using the voltage followers in Fig. 1.

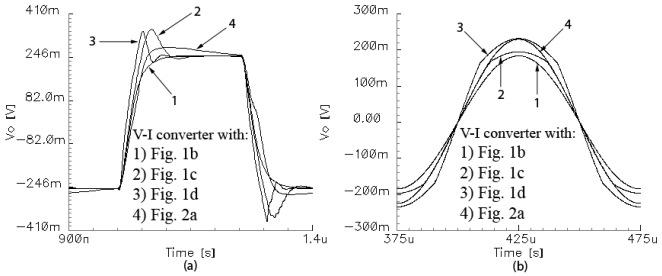

Figure 6. Transient response of the V-I converter using the voltage followers in Fig. 1 for a) a square input signal of $0.5V_{pp}$ at 2MHz and a capacitive load of C_L=15pF and b) a sine wave of $0.5V_{pp}$ at 10kHz and a resistive load of 1kΩ.

TABLE II. SLEW RATES AND LINEARITY OF THE RESULTS IN FIG. 5 USING THE V-I CONVERTER AND THE FVF'S IN FIG. 1.

FVF in Figure	*SR+ [V/µsec]*	*SR+ [V/µsec]*	*THD(%)*	*Comment*
Fig. 1b	11.5	12.5	0.15	High linearity, decreased transconductance
Fig. 1c	12.4	12.6	5.46	Decreased linearity and transconductance
Fig. 1d	13.8	13.2	8.62	Decreased linearity, high transconductance
Fig. 2a	10.3	10	0.76	High linearity and high transconductance

IV. CONCLUSION

A comparison between different approaches implementing class AB operation for the conventional basic cell denominated as Flipped Voltage Follower were presented. The discussion suggests that all architectures are suitable for high frequency operation. Additionally, a modification of conventional voltage follower to maintain a large voltage swing in the current-sourcing device was presented to support very large currents in the implementation of a class AB highly linear OTA. Simulation results in 0.5µm technology show the results of the comparison.

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