Multiple stage capacitor multiplier using dual-output differential amplifiers

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***Abstract*— A capacitor multiplier with large multiplication factor based on dual-output differential amplifiers is presented. The proposed circuit consists on multiple stages connected in series to provide a large multiplication factor, formed by transconductance differential amplifiers with dual outputs where one of the outputs provides a scaled current with respect to the other by a factor k. Simulation results in 0.5µm technology confirm the proposed operation.**

I. INTRODUCTION

Current CMOS trends on analog design require large and precise capacitors for many applications. Additionally, mobile circuitry including System-On-Chip structures demands reduced silicon area as well as decreased supply voltages and power consumption [1]. Capacitance multiplication is a well-known technique utilized to satisfy these trends. Implementations of this technique are divided in current- and voltage-mode topologies, each with its own restraints [2], [3]. Some adaptations and variations of these two basics principles have been developed up to now [4], [5].

The conventional current-mode structure presents considerable drawbacks such as narrow bandwidth and low multiplication factor. Also, they require large physical area and high power consumption. Overcoming these challenges has become an onerous task and significant efforts have been made heretofore. In this paper, we show a proposed structure that includes wide bandwidth, decreased silicon area and supply voltage. The results section shows simulation results that confirm the operation of the proposed topology.

II. COMPARED TOPOLOGIES

A. *Conventional current mirror capacitance multiplier*

The conventional current-mode structure is shown in Fig. 1(a) [5]. It consists of two transistors (Q1 and Q2), where Q2 is in diode connection, it adopts the small-signal current in C, $i_C = i_{Q2}$, and adjusts its gate-source voltage which, in parallel with Q1 induces the current i_{Q1}. If Q1 is proportionally scaled with respect to Q2 by a factor K, the induced current is also scaled, resulting in an overall current of $i_{tot} = (K+1)i_C$. The effective impedance is affected by this current; note that if a larger current is being generated by the same voltage at the output node, the impedance is decreased. Hence, the equivalent capacitance is given by

$$C_{eq}=(K+1)*C. \quad (1)$$

B. *2-OTA capacitance scaling*

The equivalent implementation of the conventional multiplier using operational transconductance differential amplifiers (OTA) is shown in Fig. 1b [2]. The amplifier OTA2 depicts a scaled transconductance gain g_{m2} with respect to g_{m1}, providing a scaled output current. The negative feedback seen at OTA1 results in an effective resistance of $1/g_{m1}$, equivalent to the diode-connected transistor Q2 in the conventional topology. The current-scaling factor is given by the ratio of the transconductance gain between OTA2 and OTA1. The equivalent capacitance is given by the same relation in (1).

This technique presents considerable drawbacks. From Fig. 1a, the multiplication factor directly depends on the scaled value between Q1 and Q2, which represents that the silicon area and power consumption is also increased by this factor, representing a notorious disadvantage.

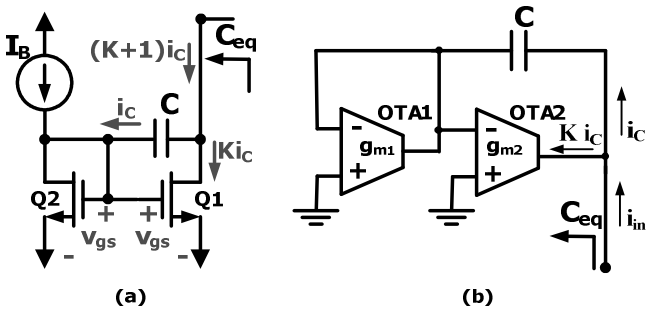

Figure 1. Conventional topologies: a) conventional current mirror capacitance multiplier and b) realization based on OTA's.

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III. PROPOSED CIRCUIT

The proposed circuit consists on connecting N number of gain stages in series, similar to the topology reported by Choi in [6], although the proposed circuit is based on differential amplifiers, which helps define the dc level to ground. The proposed circuit is shown in Fig. 2, where three gain stages are used. The amplifiers are based on the structure of a conventional OTA including a dual-output feature. Devices M6K and M8K are scaled with respect to M6 and M8, thus V_{o2} depicts an output current proportional to that of V_{o1} scaled by a factor K.

In our case, the proposed circuit consists of three stages of the conventional dual-output OTA. The output V_{o1} for each OTA is connected in negative feedback using unity gain, and the output V_{o2} is connected to the non-inverting input of the following OTA. Therefore, and considering removal of all the negative feedback loops for open-loop analysis purposes, the transfer characteristic is given by:

$$io_{OTA1} = k_1 [(gm_{2,3}) (Vi^+ - Vi^-)] \quad (2)$$

$$io_{OTA2} = k_2 [k_1 (gm_{2,3}) (Vi^+ - Vi^-)] \quad (3)$$

$$io_{OTA3} = k_1 k_2 k_3 [(gm_{2,3}) (Vi^+ - Vi^-)] \quad (4)$$

at stages 1, 2 and 3 respectively. The overall gain is given by:

$$\frac{Vout}{Vi^+ - Vi^-} = k_1 k_2 k_3 (gm_{2,3}) (rout_P \cdot rout_N) \quad (5)$$

The transient current in the capacitor is defined by $i_c = C (dV_{in} / dt)$ and the current in the second output V_{o2} is a replica of the current in the capacitor. The input current i_{in} is given by $i_{in} = (1 + k) I_c$, so the input impedance of this circuit is equal to a scaled capacitance $C_{eq} = (1 + k_1 \cdot k_2 \cdot k_3) C$, where $K = k_1 \cdot k_2 \cdot k_3$ and C is the multiplied capacitance.

IV. SIMULATION RESULTS

In order to verify the proposed circuit, simulations were performed using spectre in a 0.5µm technology, implemented in a typical RC low-pass filter. The mirroring ratio of each stage K was set to three, which results in an overall multiplication factor of 28. We used the capacitor multiplier to emulate an equivalent capacitance of 280pF using a capacitance of C=10pF. The plot in Fig. 3 shows the comparison of the simulated impedance of the proposed structure split into magnitude and phase against the ideal response. The circuit presents an effective bandwidth of ≈70kHz, an upper limit of 88dB, which corresponds to a parallel load resistance at dc of 25kΩ, and a lower limit at 34dB, which corresponds to an equivalent series resistant (ESR) of 50Ω.

The graphic illustrated in Fig. 4 shows the frequency response of the output voltage split into magnitude and phase. It exhibits a comparison between the conventional circuit in Fig. 1b and the proposed circuit in Fig. 2 implemented in a second-order LPF based on an RLC structure. The filter consists of a resistance R=10kΩ in parallel with an inductor L = 100mH, having the equivalent capacitance as a load impedance to ground, where V_{Ceq} corresponds to the output voltage.

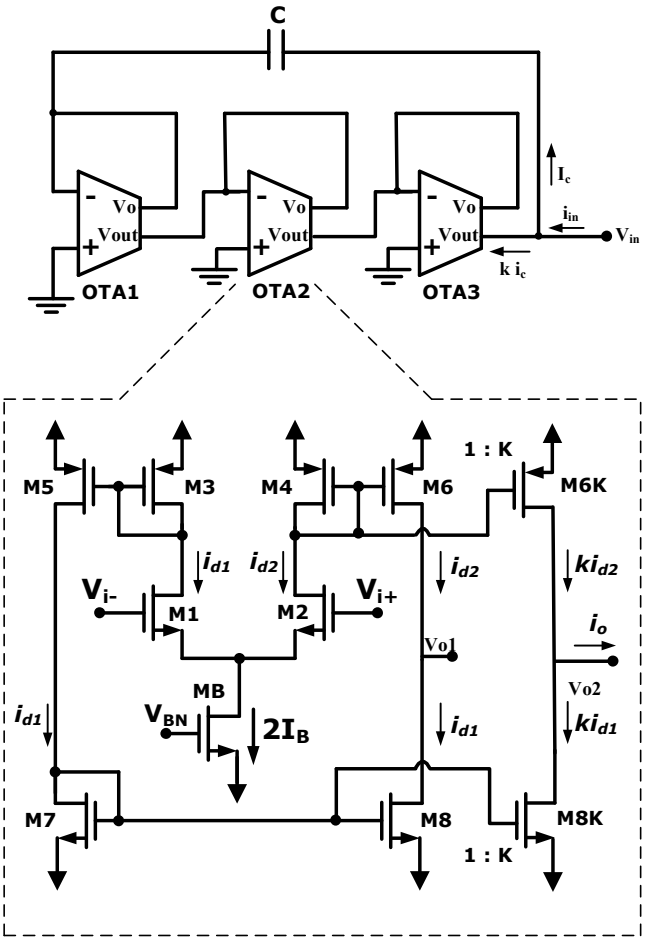

Figure 2. Proposed Circuit: 3 Stages with conventional 2-output OTA capacitor multiplier.

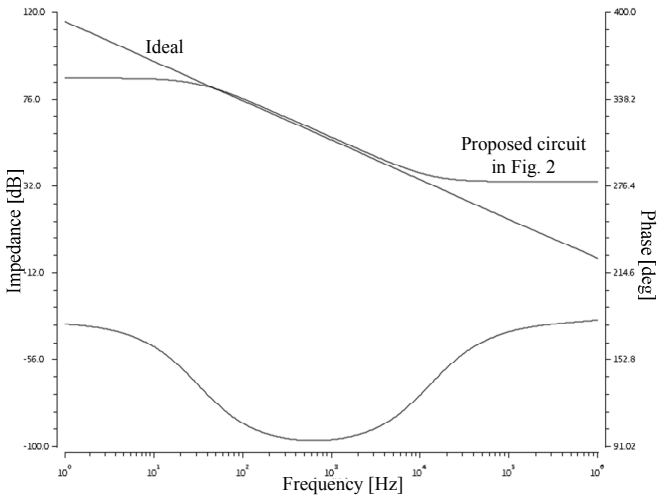

Figure 3. Compared impedance gain and bandwidth between the pasive filter and the proposed circuit.

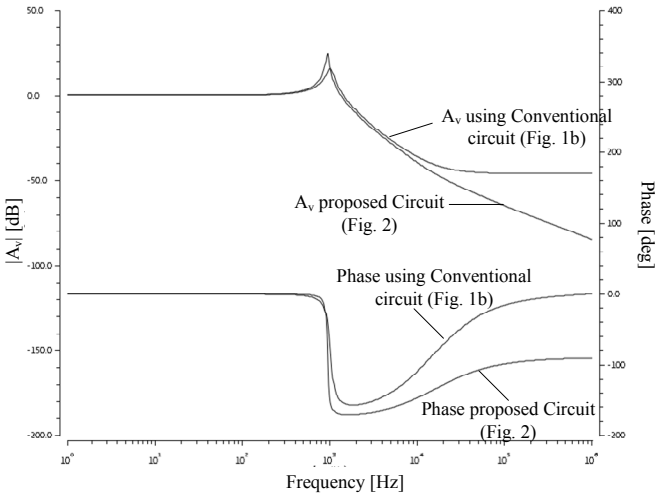

Figure 4. Compared results of the output voltage between the passive filter and the proposed circuit.

TABLE I. DESIGN PARAMETERS

Parameter	***Value***
I_B	80 µA
$V_{dd} = -V_{ss}$	2V
M1, M2, M7, M8	43.8µm / 1.2µm
MB	87.6µm / 1.2µm
M9	131.4µm / 1.2µm
M3-M6	126.6µm/0.4µm
M10	379.8µm / 1.2µm
$(V_{GS} - V_{TH})_{N,P}$	0.2 V

TABLE II. PARAMETER COMPARISON

	Conventional 2-OTA in Fig. 1b	***Proposed Circuit in Fig. 2***
Simulated THD	3.356 %	1.824 %
Power dissipation	10.88 mW	6.72 mW
Area	0.0297 mm^2	0.0171 mm^2

V. CONCLUSION

A practical implementation of an on-chip capacitor multiplier using multiple stages in series for a large multiplication factor was presented. It was shown that the implementation occupies a reduced silicon area as well as decreased power consumption. This was achieved by the design of a differential amplifier with the feature of dual outputs that offer output currents proportionally scaled by a factor K. The circuit was verified with simulation and compared with common conventional topologies

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