Final Laboratory report

Methodology used. Problems, solutions & conclusions of all the design process

Rodrigo Alcaraz Aguilar
General overview with a block diagram of the steps needed to be followed in order to create a footprint.

Procedure to create a footprint

Get the component’s datasheet

Drawing includes design of pads?

yes

Create the pad with the pad designer tool

no

Enter component drawing data in LP Calculator tool to get size of pads.

Open Orcad PCB Editor

Is the shape of the component a standard shape?

yes

Create the footprint using the “Package symbol wizard”.

Create the footprint using only the “Package symbol” menu option.

End of footprint design.
The first task to accomplish if we don't have a suggested pad size from the supplier is to enter the data in to the LP calculator in order to obtain the size of the pad and the distance between two pads which will be used for further steps.

Since we are working with mils its necessary to change the type of units every time we press the button “clear” or change the shape of the component.

Once we got the all the data needed, the next step is to create the pad. To do that, we use the Pad Designer tool.

It’s very important to be aware of the units in which we will work, in this laboratory we will use mils as a standard. And never forget the increase of size of +6 for de solder mask.

The next step after the pad has been created is to create the footprint with the Orcad PCB Editor tool.

If the component has a standard shape (ex. A resistor, qfp, sot, so etc) then we can use the package symbol wizard which is really helpful because of the time savings by using it.

Once again it's very important to define the units to work, the accuracy in case the original measures of the component were in different units in order to don’t lose it.

At this step we have to be aware of matching the reference designator prefix with the related logic library.
Once we have entered all the measures now the pad designed before has to be assigned to the footprint.

A common problem is to don’t find the pad in the menu that has already been designed; the solution is to configure all the paths to be taken into account before starting a design.

Once we choose the proper pad, (sometimes it’s useful to choose a different shape for the pin number one of a component with more than two pins to make easier the identification of that pin in particular).

After the pad was choosed, we can decide whether we want to compile or new design or not.

Some of the important things to remember at this stage of the design is to check if the order is correct or needs to be changed. To do this we have to choose the text and click in this box:

If it weren’t possible to use the wizard, then I found this tips useful dealing with the interface:

- To rotate a pin click edit->spin before choosing the pin to be erased.
- Never forget to click done after doing an action such as erasing a pin or moving a component.
- To have more accuracy when moving any element of the design in can be texted x to move something relative to the center of the component or ix relative to the center of the element selected. The same applies for the y axis with y and iy.
3-Schematic Capture

Methodology used for the schematic design:

Once libraries have been designed we can proceed with the schematic design, to do so the next tools need to be used.

1- Add a component (shortcut: “p”).

2- Wire a component with another component (shortcut “w”):

At this point is strongly recommended to have the libraries designed with pins grouped not in numerical order but in functional groups order so wiring can be much easier.

If libraries were corrected it’s necessary to update the cache otherwise changes won’t take effect on the design and even when they are updated if the
value field of the library were changed the component value in the design doesn't change.

3- Place a bus (shortcut “B”).

In order to name a bus net it is necessary to use the symbols “[ ]” e.g. “Data [15:0]”. After having drawn the bus line the next step is to connect (to wire) the pins with a bus entry (shortcut “E”).

4- Place “Power” and “Ground” (0 ground its recommended).

5- The unconnected pins should be marked with the “no connect” function (shortcut “X”).

6- The off page connectors are used to connect signals between two or more pages.

With these tools we can create the schematic. The next step after created all the pages of the schematic is to verify if there are design errors.

In the next pages of the report it will be described all the errors found in the project.
Once errors have been corrected, the next step is to create the net list (which would also show if there were warnings or errors in the design).

Finally after having created the schematic it’s recommended to check if the image of the component is shown.
List of errors corrected to get the net list:

1- No footprint associated with a padstack. Root cause: It was necessary to add that information in the "Edit Package properties menu of the corresponding part.

2- Amount of pins from the component and the padstack doesn´t match. Root cause: Less pins where declared in the footprint. Solution: Redesign the footprint or the pins declared in the footprint depending on the information shown in the datasheet.

3- Incorrect order of pins in footprints. Solution: Correct order of footprints in PCB editor according to the datasheet of the part.

4- Number of pin not declared. Root cause: design error during library parts design phase; this happened when the symbol was copied from other part. Solution: Declare the pin number in the corresponding part.
5- Possible pin type conflict. Root cause: Purpose of pins in parts not properly declared. E.g. Output Connected to Output or Output Connected to Power.

6- Problems with previous versions: Different default Orcad libraries directories. Solution: Cache needs to be replaced with the equivalent new version library. Some directories need to be updated because the folder of Orcad 16.2 doesn’t exist anymore.

**Tips**

Use of “navigating window” to debugg nets.

By double clicking the circle net listing errors appears with green circles.

To change libraries after their creation.
4- PCB Layout

Forward annotation of netlist using the “Calvin Board Template” as the input file to generate the .brd file to be used in PCB Editor

The session log shows the warnings and errors of the schematic design.

At this laboratory there were no errors but lots of warnings. Most of them were caused because of a different character in a name of a net and missing adding the name of each net in the bus (It’s not only necessary to name the bus but also every single net).

----- Summary Statistics -----  
No error detected  
No oversight detected  
No warning detected
The project was optimized until no warnings and errors were found. To do so, it was very useful the “Net List report” generated in the “Allegro PCB design” interface.

Verify the Layer Stack Up

In this laboratory, it was used the Calvin template which includes the following layer stack up.

<table>
<thead>
<tr>
<th>PCB Stack-up</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Layer type</strong></td>
</tr>
<tr>
<td>Signal</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Plane</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Signal</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Signal</td>
</tr>
<tr>
<td>Plane</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>Signal</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

To verify that the stack up is ok it is necessary to use the Cross-Section utility where more layers can be added and all the stack up characteristics are defined.
Set DFA component spacing requirements

The DFA component spacing suggested is 20 mils.

In order to define the component spacing there is a matrix where the spacing between all the components is defined. In this case the 20 mils value was applied simultaneously to all the components.
Component Placement

As it was mentioned in the introduction, the component placement is even considered by some experts to be the 90% of a PCB design.

In this laboratory a suggested placement was used for the top side.

I’d like to add some very good suggestions from the PCB design tutorial explained in class because it was very helpful to save time from the beginning to avoiding mistakes.

- Set your snap grid, visible grid, and default track/pad sizes.
- Throw down all the components onto the board.
- Divide and place your components into functional “building blocks” where possible.
- Identify layout critical tracks on your circuit and route them first.
- Place and route each building block separately, off the board.
- Move completed building blocks into position on your main board.
- Route the remaining signal and power connections between blocks.
- Do a general “tidy up” of the board.
- Do a Design Rule Check.
- Get someone to check it.

In my case, since I was using the Calvin suggested placement for top side, I preferred not to add all the components at the same time to the design, but to add one by one.

The steps to do the placement are shown in the next figures:
The components will be placed automatically in the top side but if it is required to place a component in the bottom side it's necessary to mirror the component as the next figure shows:

Once a component is placed, the reference in the “Place Manually” dialogue box will appear in yellow with a letter P.

The next figure shows the placement completed for both sides:

Once there are no components left, the next step is to enter the physical, spacing and electrical constraints.
Physical, Spacing and Electrical routing constraints

In order to set the physical, spacing and electrical routing constraints it is necessary to run the constraint manager.

These constraints must be set before the routing is started.

The type of constraint to be set can be chosen with the worksheet selector.

For physical constraints:

Physical constraints groups are created:
Inside these groups we will assign the value suggested in the Calvin constraint reference document for each layer as this example shows (this part already came with the template):

<table>
<thead>
<tr>
<th>Type</th>
<th>Differential Pair</th>
<th>(+)Tolerance</th>
<th>(-)Tolerance</th>
<th>Vias</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dan</td>
<td>laboratory_5</td>
<td>0.00</td>
<td>0.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>PCS</td>
<td>DEFAULT</td>
<td>0.00</td>
<td>0.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>PCS</td>
<td>DIFFERENTIAL</td>
<td>0.00</td>
<td>0.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>Lyr</td>
<td>TOP</td>
<td>5.00</td>
<td>5.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>Lyr</td>
<td>L2_GND</td>
<td>5.00</td>
<td>5.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>Lyr</td>
<td>L3</td>
<td>5.00</td>
<td>5.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>Lyr</td>
<td>L5_PWR</td>
<td>5.00</td>
<td>5.00</td>
<td>VIA_20-10</td>
</tr>
<tr>
<td>Lyr</td>
<td>BOTTOM</td>
<td>5.00</td>
<td>5.00</td>
<td>VIA_20-10</td>
</tr>
</tbody>
</table>

To choose a type of via it’s necessary to double click in the fields of the “vias” column and choose a via previously added in the padstack folder.
All the nets will be divided into classes in order to add different characteristic to each type of class.

E.g. “Memory data”, power, spi_clk, etc.

And it will be selected a referenced physical Cset (previously declared) to each class.

Also the neck constraint is set in this section. This constraint helps to have the possibility to do thinner lines for example for a power line in a fine pitch IC that touches other pins.
For spacing constraints:

Just as it was created a physical set in the last section, in this section we will create several spacing constraints which later will be assigned to a net class.
The next step is to create spacing constraints between net classes.

For electrical constraints:

For propagation delay we create a match group that consist in a target signals and other signals related that must match in the length with certain tolerance.
After the match group is created, then the membership of the signals which will be related need to be added in the match group membership.

E.g.

Once the match group is completed the next step is to set the target and the tolerances.
Finally we will set a total etch length electrical constraint.

This can be typed directly in the total etch length menu or configured previously with an electrical constraint.

This takes us to the end of the constraints configuration.
Routing of all signals/nets

An orthogonal routing strategy was chosen to route this project. The next tools were used to route in Allegro:

- General edit: Allows to choose shapes in order to move, delete, etc.
- Etch edit: This tool automatically activates or starts a Cline.
- Placement edit: This tool automatically activates to pick a complete component in order to move it.
- Add connect: This tool activates or starts a Cline when a pin is clicked.
- Slide: This tool helps to move a placed Cline.
- Delay tune: This tool helps to make automatically longer a line for tuning propagation delays.
- Custom smooth: This tool helps to smooth traces with many curves.
- Create fan-out: This tool helps to create automatically fannouts even for several pins at the same time.
- Unrats all: This tool hides the not yet routed nets.
- Rats all: This tool shows all the unconnected nets.
- Color 192: This tool helps to show or hide the different layers. It was very useful to use F4 (show element) to see where certain shape, net, pin, etc was placed in order to hide it with the color 192 toll.
- **Find:** It is only possible to select the checked boxes. This helps a lot when an element is over or under other element.

- **Options:** This tool changes depending on what activity is being done. I'll describe the most common.

When routing, the options tables let us choose which layer is active and to which layer the Cline will change.

- **The change tool is used when a font of a text or change of layer of an element is needed.**
Visibility: This tool helps to choose which layers and which elements need to be shown in the screen. The “view” option let us activate different configurations of elements to be shown.

The right click when routing opens a wide variety of useful options. I’ll explain some of the most common utilized in this laboratory.

- Add Via: adds a via. This can be done faster by double clicking when routing.
- Change active layer: This helps to move from one layer to another, before chance we need a via, otherwise it won’t be possible to change the active layer.
- Change alternative layer: Is the layer that is activated when a via is placed.
- Neck mode: makes the line thinner for a certain length configured in the constraint manager. Neck mode helps to avoid touching pins in a fine pitch component when the line is wider than the pitch.
- Options:
  - Shove vias: pushes the vias when routing.
  - Bubble: Lets choose between shove or hug vias.
DCRs

Once the design is finished it is time to check the DRCs.

I'll list the errors done in this design. Before doing this it is recommended to update the DRCs list.

1. For some reason the line with constraint was updated later, so some nets where thinner. This was corrected by double clicking in the line with the error with the “slide” tool (shift+F3).
2. Vias overlapping.
3. Total etch length not enough.
4. Propagation delay not tuned.

Status of the design

The lists of DRC errors appear by clicking in the DRC errors box. If this box is in red, this means that a change was done and it is necessary to click the “update DRC” box.
5- Fabrication Files

IPC-356 Netlist

SUMMARY:
Errors: 0
Warnings: 10

Fabrication Drawing

Page border
**Fabrication notes**

<table>
<thead>
<tr>
<th>Fabrication notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Productivity Level: IPC-2221A Level 3.</td>
</tr>
<tr>
<td>2. Materials: Copper foil and prepreg shall be in accordance with IPC-NF-150.</td>
</tr>
<tr>
<td>Copper foil shall be in accordance with IPC-NF-150.</td>
</tr>
<tr>
<td>3. Finish: Silk screen shall be white permanent and non-conductive.</td>
</tr>
<tr>
<td>4. Manufacturer identification and part code letter shall be rendered on the bottom side of the board.</td>
</tr>
<tr>
<td>5. Test requirements: 100% test list electrical verification.</td>
</tr>
</tbody>
</table>

**Stackup drawing**

**Drill File (listing the x-y coordinates of all drills and tools used)**
Gerber Files

To generate the gerber files it necessary to generate all the artworks required.

For some artworks, some new sub-classes are needed.
In my case I had two warnings every time I open the Artwork control form.

To solve these problems it was necessary to verify the gerber format, and the integer and decimal places.

The reference designators are aligned in the assembly and silkscreen layers.
Finally, the artwork is going to be created.

But this error appeared

So the db doctor was used solve this problem.
The design was completed and with no errors
Finally only with the intention of checking the artworks the GC-prevue program was used as follows.
Conclusions

In this course I learned that the process of designing a board is very complex since the design has to be done not only considering the proper electrical functioning of a device, but also considering manufacturing issues.

I think that the topics schedule set in the beginning of the semester was successfully fulfilled. I find very useful all the tools learned in this course for further use in the following courses.